

**REMARKS**

The Office Action indicated that claims 10, 11 and 13-16 were rejected under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter. Claims 1-9 and 12 were rejected under 35 U.S.C. § 103(a) as being allegedly obvious over U.S. Patent No. 6,151,663 ("Pawlowski") in view of U.S. Patent No. 6,377,640 B2 ("Trans"). These rejections are respectfully traversed, for reasons including those set forth below.

***Rejections of Claims 10, 11 and 13-16 Under 35 U.S.C. § 101***

Regarding claim 10, the Office Action stated the following: "Claim 10 cites 'processor masks' with no mention of physical or logical relationship between elements, designed to support interconnection controller functions." Actually, claim 10 recites "semiconductor processing masks," the use of which is well known to those of skill in the art. However, in order to expedite the processing of this application, claim 10 has been amended to recite that the set of semiconductor processing masks is "configured for fabricating, at least in part, the integrated circuit of claim [[6]] 9." (*Id.* at p. 2, lines 11-13.) This amendment further clarifies the physical and logical relationship between the semiconductor processing masks and those of the interconnection controller, which is embodied in an integrated circuit in this example.

Regarding claim 11 and 13-16, the Office Action indicates the following:

Claim 11 cites "data structures" with no mention of physical or logical relationship among data elements, designed to support specific data manipulation functions. Therefore, "data structures" is deemed non-statutory and rejected under 35 U.S.C. 101. Claims 13-16 are thereby rejected secondary to their dependence upon claim 11.

(*Id.* at p. 2, lines 14-17.)

The U.S. Patent and Trademark Office's "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" ("USPTO Guidelines") state the following regarding data structures:

Data structures not claimed as embodied in computer-readable media are descriptive material *per se* and are not statutory because they are not capable of causing functional change in the computer. See, e.g., *Warmerdam*, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure *per se* held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. *In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.*

(*Id.* at p. 52, last paragraph [emphasis added].)

Similarly, the USPTO Guidelines note: "When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized." (*Id.* at p. 50, second paragraph.)

These general rules apply here. Claim 11 recites "At least one computer-readable medium having data structures stored therein representative of the interconnection controller of claim 6." The data structures of claim 11 may comprise, for example, a code description (see claim 14) for implementing the functionality of the interconnection controller recited in claim 6, e.g.:

perform[ing] an initialization sequence with the non-local interconnection controller that establishes a characteristic skew pattern between data lanes of the point-to-point inter-cluster links;

recover[ing] clock data from symbols received on the point-to-point inter-cluster links; and

apply[ing] the characteristic skew pattern to correct for skew between data lanes of the point-to-point inter-cluster links.

The claimed data structures are recorded on a computer-readable medium and permit this functionality to be realized. Accordingly, the data structures of claim 11 and 13-16 are statutory subject matter according to the controlling case law and the USPTO Guidelines.

***Rejections of Claims 1-9 and 12 Under 35 U.S.C. § 103(a)***

The Background section of the present application notes the following:

A relatively new approach to the design of multi-processor systems *replaces broadcast communication such as bus or ring architectures* among processors with a point-to-point data transfer mechanism in which the processors communicate similarly to network nodes in a tightly-coupled computing system. That is, the processors are interconnected via a plurality of communication links and requests are transferred among the processors over the links according to routing tables associated with each processor. The intent is to increase the amount of information transmitted within a multi-processor platform per unit time.

In some multi-processor systems, local nodes (including processors and an interconnection controller) are directly connected to each other through a plurality of point-to-point intra-cluster links to form a cluster of processors. Separate clusters of processors can be connected via point-to-point inter-cluster links. The point-to-point links significantly increase the bandwidth for coprocessing and multiprocessing functions.

(*Id.* at p. 1, line 22 through p. 2, line 8 [emphasis added].)

The present application addresses certain challenges of implementing multi-processor systems having point-to-point data transfer mechanisms instead of bus-based data transfer mechanisms or the like: “[u]sing a point-to-point architecture to connect multiple processors in a multiple cluster system presents its own problems.” (*Id.* at p. 2, lines 8-10.)

Accordingly, the computer system of independent claim 1 recites:

a first cluster including a first plurality of processors and a first interconnection controller, *the first plurality of processors and the first interconnection controller interconnected by first point-to-point intra-cluster links; and*

a second cluster including a second plurality of processors and a second interconnection controller, *the second plurality of processors and the second interconnection controller interconnected by second point-to-point intra-cluster links, the first interconnection controller coupled to the second interconnection controller by point-to-point inter-cluster links . . .*

(Emphasis added.)

Similarly, independent claim 6 recites “a plurality of local processors arranged in a point-to-point architecture in a local cluster” and “point-to-point inter-cluster links.”

The Office Action asserts that these features are disclosed in the Pawlowski patent. (See, e.g., Pawlowski at p. 3, lines 4-17 and p. 5, lines 8-15.) However, as understood, Pawlowski does not teach, suggest or indicate the use of point-to-point intra-cluster links or point-to-point inter-cluster links. The nodes within the clusters described in Pawlowski are connected by a “local cluster CPU bus.” (See, e.g., Pawlowski at Figure 1 and col. 2, line 64 through col. 3, line 1.) Likewise, “[t]he clusters 10 are coupled together by an inter-cluster system bus 20, which bus is also coupled to an inter-cluster system controller.” (Id. at col. 3, lines 10 and 11.)

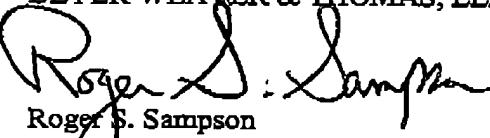
Therefore, it is respectfully submitted that claims 1 and 6 are allowable over the art relied upon. Because all claims in the application depend from claim 1 or 6, all other claims are also allowable.

**CONCLUSION**

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

The Commissioner is hereby authorized to charge any additional fees, including any extension fees, which may be required or credit any overpayment directly to the account of the undersigned, No. 50-0388 (Order No. NWISP041).

Respectfully submitted,  
BEYER WEAVER & THOMAS, LLP



Roger S. Sampson  
Reg. No. 44,314

P.O. Box 70250  
Oakland, CA 94612-0250  
(510) 663-1100